ABSTRACT

[0032] A device for implementing transaction ordering enforcement between different queues of a computer system interconnect using an inter-queue ordering mechanism. The device includes first and second circular queues and input and output counters. The queues have an ordering dependency requirement between them such that entries in the second queue are not allowed to pass entries in the first queue. One requirement is that an entry in the second queue cannot be dequeued before an entry that was placed earlier in the first queue is dequeued. Another requirement is that an entry in the second queue cannot be dequeued before an entry that was placed earlier in the first queue is dequeued and then acknowledged as completed. The input and the output counters increment whenever an entry is enqueued to or dequeued from the first queue, respectively. The device may be implemented PCI and PCI-X systems or other interconnect systems.